ECE-347  ELECTRONICS+LAB

FINAL EXAM  16.01.2012

This is a closed-book, closed-notebook exam. You can use an A3 with full of your hand-written notes. No photocopy even partial is accepted. Calculator can be used. No mobile device (phone, laptop, ipod etc.).

There are 8 questions. Total 100 points.

Exam duration is 2 hours. Print your number and name on every page. Use the back of the pages for your answers.

1. (20p) In the differential amplifier circuit given a current-mirror circuit is used to perform a current source.
Calculate
a) The differential gain (A_{dd})

b) The common-mode gain (A_{cm}).

$Q_1, Q_2, Q_3, Q_4$ are identical.
$V_{BE} = 0.7V, \ V_T = 26mV.$
(20p) For the op-amp active filter circuit given:
   a) Calculate the cut-off frequencies.
   b) Calculate the mid-frequency voltage gain \( \text{Av} = \frac{Uo}{Ui} \).
   c) Draw the Bode plot for the circuit.

(3)

Two feedback circuits are given as

(10p)

a) What type of feedback circuits are these? Write the feedback gain \( (B) \) for each of the circuits.

b) Calculate the input impedances \( (2i) \) of these circuits.
(4) The ladder network below is given.

\[ \begin{align*}
R & \quad R \\
2R & \quad 2R \\
\text{V(0)} & \quad \text{V(1)}
\end{align*} \]

a) Is this a Digital to Analog Converter (DAC) circuit or Analog to Digital Converter (ADC) circuit?

b) What is the number of bits converted by this circuit?

c) If V(0) = 0V and V(1) = 5V then calculate Vo.

d) What is the resolution of this circuit?

(5) A successive approximation register (SAR) analog to digital converter (ADC) is given below.

\[ \text{Sampling fs} \]

\[ \text{Comparator} \quad \text{Control} \quad \text{SAR} \quad \text{DAC} \]

\[ \text{fosc = 40 kHz} \]

\[ \text{Up, down} \]

\[ \text{02, 01, 00} \]

\[ \text{analog out} \]
a) Explain how this circuit works?

b) If analog input signal is \( u_{\text{in}} = 3 \sin 2\pi 10^4 t \)

(I) Calculate the resolution of the ADC.

(II) What should be the minimum frequency (fs) to sample this signal? Explain.

(III) If the SAR catches the input signal sample in 3 clock cycles on the average, how long it takes to convert a sample into digital?

(IV) How long will it take 1 digital word \( (Q2, Q1, Q0) \) to be sent serially with the same clock?

(5) In the op-amp circuit, show that

\[ u_0 = \left(1 + \frac{R_2}{R_1}\right)(u_1-u_2). \]
7. Calculate $u_0$ and simplify the result.

8. What type of a linear integrated circuit (IC) you must properly use for the application?

   a) Summing 3 signals
   b) Integrating an input signal
   c) Frequency demodulation
   d) An oscillator of frequency changing with input signal
   e) Taking derivative of the signal
f) multiplying the input signal frequency

g) A clock signal that can be used for digital counters

h) A clock signal whose frequency can be set by external resistors and a capacitor
In the differential amplifier circuit given above, a current mirror circuit is used to perform as a current source. Calculate:

a) The differential gain \((A_{vd})\)
b) The Common-mode gain \((A_{cm})\).

\[ A_{vd} = \frac{R_c}{2R_e} \]  \hspace{1cm} a) \hspace{0.5cm} R_e = \frac{V_t}{I_E} \]

\[ A_{cm} = \frac{-R_c}{2R_e + R_E} \]  \hspace{1cm} \text{at Q2's base: } V_{BE} = 0 \text{V. (Connected to the ground)}

\[ V_{BE} = 0 \text{V, } V_{BE} = -0.7 \text{V, } V_{BE} = -1.4 \text{V.} \]

\[ I_{E2} = I_{E4} = \frac{-1.4 \text{V} - (-V_{EE})}{R_P} \]
\[ I_{E2} = I_{E4} = \frac{-1.4 - (-10)}{2 \times 10^3} = \frac{8.6}{2 \times 10^3} = 4.3 \text{ mA} \] (5)

\[ I_{E1} = I_{E3} = 4.3 \text{ mA} \quad \text{(because } \beta_3 \text{'s and } \beta_4 \text{'s } V_{BE} \text{'s are the same)} \]

\[ A_v = -\frac{R_c}{2R_e} \]

\[ A_v = -\frac{2 \times 10^3}{2 \times 6} = -170 \] (2)

\[ R_e = \frac{V_I}{I_E} = \frac{26 \text{ mV}}{4.3 \text{ mA}} = \frac{26}{4.3} \Omega \]

\[ b) \quad A_{VCM} = -\frac{R_c}{R_e + R_E} \]

Since the current mirror is a current source, the

\[ R_E \to \infty \]

\[ A_{VCM} = -\frac{2 \times 10^3}{6 + \infty} = 0 \] (4)
For the op-amp active filter circuit given:

a) Calculate the cutoff frequencies
b) Calculate the mid-frequency voltage gain \((A_e = \frac{U_o}{U_i})\)
c) Draw the Bode Plot for the circuit.

\[\text{Diagram of the circuit}\]

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50Ω

\[10\text{K} \quad 50\text{K}\]

\[40\text{K} \quad 10\text{K} \quad 1\text{K}\]

\[1\text{K} \quad 400\text{pF}\]

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\[\text{Solution}\]

a) 1st op-amp circuit is a low-pass filter.
\[
fc_1 = \frac{1}{2\pi \times 1\text{K} \times (400\text{pF})} = \frac{1}{2\pi \times 10^3 \times 4 \times 10^{-12}} \approx 4 \times 10^5 \text{ Hz} = 400\text{KHz} \tag{4}
\]

2nd op-amp circuit is a high-pass filter.
\[
fc_2 = \frac{1}{2\pi \times 1\text{K} \times 10^3} \approx 80 \text{ Hz} \tag{4}
\]

b) The mid-frequency voltage gain is
\[
A_e = \left( 1 + \frac{90}{10} \right) \left( 1 + \frac{50}{15} \right) = 10 \times 5 = 50 \tag{4}
\]

c) The Bode Plot for the circuit is shown with relevant asymptotes and frequency labels.
Two feedback circuits are given as

![Feedback Circuits](image)

(I) \hspace{2cm} (II)

a) What types of feedback circuits are these? Write \( B \) for each of them.

b) Calculate the input impedances of these circuits.

**Sol:**

a) I: Voltage series feedback circuit. \( B_1 = \frac{v_f}{v_o} = \frac{R_1}{R_1 + R_2} \)

II: Voltage shunt feedback \( B_2 = \frac{i_f}{i_o} = \frac{V_o/R_2}{V_o} = \frac{1}{R_2} \)

b) I \( \Rightarrow Z_f = Z (1 + BA) = Z (1 + 1000) \to \infty \)

II \( \Rightarrow Z_f = \frac{Z_1}{1 + BA} = \frac{Z_1}{1 + \frac{1}{R_2} \infty} = \frac{\infty}{1 + \frac{1}{R_2} \infty} \)

Open-loop impedance of op-amp \( \infty \)

\[ Z_{\text{op-amp}} = R_2 = \frac{V_o}{I_{\text{in}}} \]
The ladder network below is given.

a) Is this a Digital to Analog Converter (DAC) circuit or Analog to Digital Converter (ADC) circuit?

b) What is the number of bits converted by this circuit?

c) If \( V(0) = 0V \) and \( V(1) = 5V \) then calculate \( U_0 \).

d) What is the resolution of this circuit?

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**Solution**

a) This is a DAC

b) 2 bits

c) 

\[
\begin{align*}
U_0 &= \frac{5V}{4R} \\
U_0 &= 1.25V
\end{align*}
\]

d) Resolution is 1.25V
A successive approximation register (SAR) analog-to-digital converter (ADC) is given below.

\[ f_{osc} = 40 \text{kHz} \]

\[ \text{ADC} \]

\[ Q_2 \rightarrow Q_1 \rightarrow Q_0 \]

\[ \text{DAC} \]

Digital out

a) Explain how the circuit works.

b) If analog input signal is \( u_{in} = 3 \sin 2\pi 10^4 t \) -

i) Calculate the resolution of the ADC. 

ii) What should be the minimum frequency to sample this signal? Explain.

iii) If the SAR catches the input sample in 3 clock cycles on the average, how long does it take to convert a sample into digital?

iv) How long will it take 1 digital word in a verse line with the same clock?

**SOL:**

When a sample of the signal is taken, the comparator compares this analog signal sample with the signal at its other input, which is obtained from the DAC. The SAR first tries the middle voltage value.

\[
\frac{2 \times 3V}{2^{3-1}} = \frac{6}{2} = 3 \text{V}
\]

\[
5.142 < \text{middle} < 3.428 \text{V}
\]

\[
1 \rightarrow 0 \text{ 1st step}, 0 \rightarrow 1 \text{ 2nd step, } 1 \rightarrow 0 \text{ 3rd step}
\]
Until it catches the signal. When it catches the signal, this value is converted by the DAC to analog and sent to the comparator. Since this voltage is more or less equal the input signal, then the comparator changes state and it stops the SAR. At this instant the digital signal at the output of the SAR is the converted digital signal.

(1) Resolution of the ADC = \( \frac{6V}{2^{7-1}} = \frac{6V}{4} = 0.857 V \)  \( \circ \)

(II) \( f_s \geq 2 f_{signal} \) (Nyquist criterion)

\( f_s \geq 2 \times 10^4 \text{ Hz} \)  \( \circ \)

(III) If it takes 3 clock cycles to catch the analog signal then

we have \( 3 \times T_{\text{clock}} = 3 \times \frac{1}{40 \text{kHz}} = \frac{3}{40 \times 10^{-3}} = 75 \times 10^{-3} \)

\( = 75 \times 10^6 \text{ sec} = 75 \mu s \)  \( \circ \)

(IV) Since we have 3 bits in each digital word, it takes 3 clock cycles to send this word on a line in series.

\( 3 \times 75 \mu s = 225 \mu s \)  \( \circ \)

It takes 225 \( \mu s \) to send 1 word of 3 bits in series on a wire.
In the op-amp circuit, show that

\[ V_0 = \left(1 + \frac{R_2}{R_1}\right)(V_1 - V_2) \]

![Diagram of the op-amp circuit](image)

**Solution**

\[ I = \frac{V_0 - V_1}{R_2} = \frac{V_1 - V_2}{R_1} \]

\[ V_L = \frac{V_0}{R_1 + R_2} \cdot R_2 \]

\[ V_0 = V_1 \left(\frac{R_1 + R_2}{R_2}\right) \]

\[ \frac{V_0 - V_1}{R_2} = \frac{V_1 - V_2 \left(\frac{R_1 + R_2}{R_2}\right)}{R_1} \]

\[ \frac{V_0}{R_2} = \frac{V_1}{R_2} + \frac{V_1}{R_1} - V_2 \left(\frac{R_1 + R_2}{R_1 R_2}\right) \]

\[ V_0 = \frac{V_1 (R_1 + R_2)}{R_1 R_2} - V_2 \left(\frac{R_1 + R_2}{R_1 R_2}\right) \]

\[ \frac{V_0}{R_2} = \left(\frac{R_1 + R_2}{R_1 R_2}\right) (V_1 - V_2) = \left(1 + \frac{R_2}{R_1}\right)(V_1 - V_2) \]
Solve: \[ u_{d1} = u_1 - u_2 \] \[ u_{d2} = u_1 \] \[ u_{o3} = u_2 \left(1 + \frac{3R}{5R}\right) = 4u_2 \] These are inputs to the summing amplifier.

\[ u_o = -10R \left(\frac{(u_1 - u_2)}{2R} + \frac{u_1}{R} + \frac{4u_2}{5R}\right) \]

\[ u_o = -5(u_1 - u_2) - 10u_1 - 8u_2 \]

\[ u_o = -5u_1 + 5u_2 - 10u_1 - 8u_2 \]

\[ u_o = -15u_1 - 3u_2 \]

\[ u_o = -3 \left(5u_1 + u_2\right) \]
What type of a linear integrated circuit you most properly use for the application:

a) summing 3 signals: \( \text{Op-amp} \)

b) integrating an input signal: \( \text{Op-amp} \)

c) frequency demodulation: \( \text{PLL} \)

d) An oscillator of frequency changing with input signal: \( \text{VCO} \)

e) taking derivative of the signal: \( \text{Op-amp} \)

f) multiplying the input signal frequency: \( \text{PLL} \)

g) a clock signal that can be used for digital counters: \( \text{Timer} \)

h) a clock signal whose frequency can be set by external resistors and a capacitor: \( \text{555} \)